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Chaos: A Nonlinear Phenomenon in AC-DC Power-Factor-Corrected Boost Convertor

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Abstract: Nonlinear Dynamics is a very popular topic for researchers. The prior researchers already studied the nonlinear dynamics of current controlled DC-DC boost converter. The power factor corrected boost regulator is a circuit which is designed especially as input power factor can maintain unity. Firstly, we derive the state equations of this switching circuit. The circuit is numerically simulated by MATLAB Simulink module. Here load resistance is taken the major parameter for observing the system dynamics. The fundamental, subharmonic, and chaotic orbits are reported after getting simulation results. The paper also proposes a control system that automatically stabilizes one-dimensional time-delayed chaotic system. The delayed-feedback control (DFC) is proposed to stabilize the unstable periodic orbit (UPO) as it is not accepted for designing the practical power supply.

Keywords: PFC Boost Regulator; State Equations; Phase-Plane Trajectories; Chaos; Chaos Control.

I. INTRODUCTION

The studies of complex behaviour in switching power converters have gained increasingly more attention from both the academic community and the industry. This switched ac-dc power factor correction boost converter [1] provides dc voltage at the output end with having high input power factor. A low power factor decreases the power level in the utility grid, with a high harmonic distortion to the line current that causes EMI problems. It is usually assumed ripple free output by considering a huge output capacitor to load side, which is not acceptable in design due its bulky size and cost. Thus this system is designed to ensure a minimum distortion and circuits used to achieve unity power.

Various kinds of nonlinear phenomena, such as bifurcation and chaos have been revealed [2][3]. Chaos could be described as noise like, bounded oscillations with an infinite period found in nonlinear, deterministic systems [4]. These complex behaviours implying instability can be observed by changing circuit parameters. The occurrence of bifurcation and chaos in power electronics was first reported in the literature in the late80's [5][6].

The route to chaos in a current controlled boost converter was first discussed by Deane [7]. Chan and Tse [8], S. Banarjee and K. Chakrabarty [9] studied various types of routes to chaos and their dependence upon the choice of bifurcation parameters. The nonlinear dynamics of PFC boost converter has been reported [10].

The prior researchers described the control of Chaos depending on small, time-dependent parameter or input perturbations [11] [12]. Some other different strategies to control chaotic dynamics have been proposed in recent surveys [13], [14], [15]. Pyragas proposed *Time-Delayed Auto Synchronization (TDAS)* [16]. Socolar reported *Extended Time-Delayed Auto Synchronization (ETDAS)*[17].

In this paper, the power-factor-correction boost convertor is considered continuous conduction mode to analyse its nonlinear behaviours. Firstly, the designing and simulation aspects of current-mode controlled *pfc* boost

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convertor are operating in chaotic regime. Secondly, is used to chaos controller to control the chaotic region.

II. Circuit Designing Concept

In power-factor-correction converter the input line voltage and current are in almost same phase (*i.e.* unity *pf*) with considering almost ripple free output voltage. Here active circuit of utility interference is designed for shaping the input line current by using power electronic converter.

Based on these considerations, $v_C > V_{in}$, where V_{in} is the peak of the ac input voltage v_{in}. Therefore, the obvious choice for the current shaping circuit is a step-up ac-dc converter. The output capacitor, C_d is designed to minimize the output voltage ripple in v_C. Because the input current to the step-up converter is to be shaped, the step-up converter is operated in a current-regulated mode. The feedback control is shown in a block diagram form in Fig. 1, where $i_L^*(reference)$ is the reference or the desired value of the current $i_L(actual)$. The amplitude of $i_L^*(reference)$ should be maintained by multiplier block. The error voltage v_e from the Error Amplifier 2 then is fed to the multiplier and multiplied with input voltage to get the $i_L^*(reference)$. The error i_e that is the output of Error Amplifier1, as the difference of $i_L(actual)$ and $i_L^*(reference)$ provides the correct timing logic for the switching driver circuit to turn on and off the Boost converter (Only *Constant-Frequency Control* is considered).

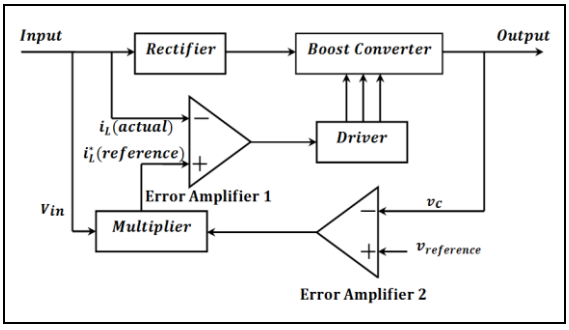

Fig. 1. PFC control strategy block diagram [1]

III. State Equations

The two pairs of state equations [1] of the circuit depending on state of the power switch. When switch is closed, the inductor current rises with ignoring any clock pulse arriving during that period. The switch opens when current reaches the reference current. When switch is open, the current falls until the arrival of next clock pulse.

1). The State Equations during "ON" period

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{in}}{L} \\ \dfrac{dv_C}{dt} = -\dfrac{v_C}{RC} \end{cases} \quad (1)$$

2). The State Equations during "OFF" period

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{in}}{L} - \dfrac{v_C}{L} \\ \dfrac{dv_C}{dt} = \dfrac{Ri_L - v_C}{RC} \end{cases} \quad (2)$$

Where,

V_{in} = Input Voltage, L = Inductor, C = Capacitor,
i_L = Inductor Current, v_C = Capacitor Voltage.

IV. Proposed Model

Many prior researchers investigated the current-mode control dc-dc boost converter with considering linearized models. Those circumstances some assumptions implied to direct the system toward linear models[1]. They assumed that the output ripple is neglected by using a huge output capacitor, which is not acceptable in design due to its bulky cost and size. Also the input time-varying voltage was replaced with its root mean square (rms). With taking all these assumptions, the linear system was derived ignoring the effect of nonlinearity, introduce a small-signal equivalent circuit, and discussed the stability problem depending on these linear treatments. The main feature of this *pfc* circuit is the use of a multiplier that introduces its nonlinearity. The circuit modelling and simulation are done by MATLAB (Fig. 2).

V. Phase Plane Trajectories

The Simulation model is totally designed by Simulink blocks. The phase-plane trajectory is constructed between the output capacitor voltage v_C and the inductor current i_L. The phase-plane trajectories are shown below.

TABLE I: Values for System Parameters

Symbol	Quantity	Designed Values for Parameters
v_{in}	Input Voltage	$220\sqrt{2}\sin\omega t\ Volt$
L	Inductor	$40mH$
C	Capacitor	$100\mu F$
f_s	Switching Frequency (SW)	$20kHz$
R	Load Resistance	35Ω / 45Ω / 67Ω

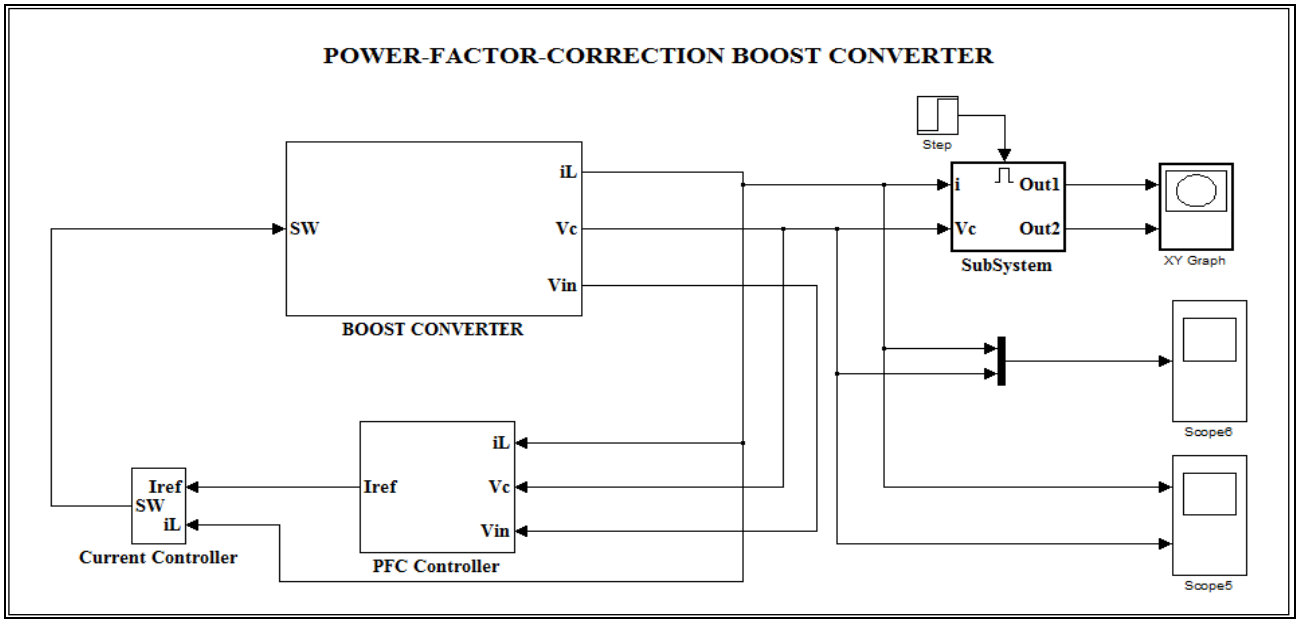

Fig. 2. Boost PFC ac-dc regulator under fixed frequency current mode control. [1]

Diagrams of Phase-Plane Trajectories

A. Case I(Period I Operation)

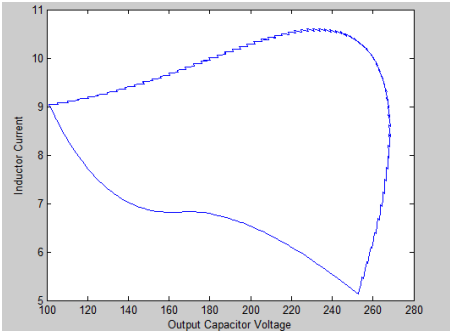

Fig. 3. Phase Plane Trajectory (Case I) [1]
Capacitor Voltage vs. Inductor Current (Period I operation)

B. Case II(Period II Operation)

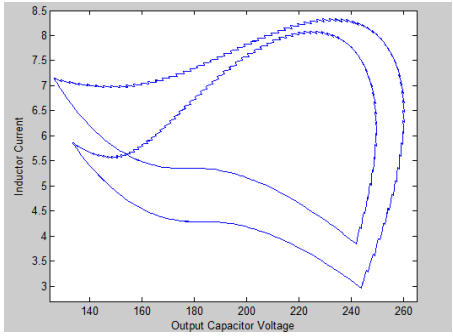

Fig. 4. Phase Plane Trajectory (Case II) [1]
Capacitor Voltage vs. Inductor Current (Period II operation)

C. Case III(Chaotic Mode Operation)

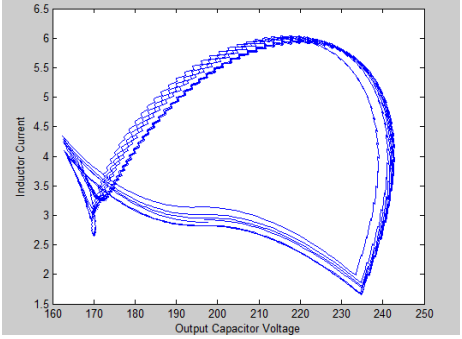

Fig. 5. Phase Plane Trajectory (Case III) [1]
Capacitor Voltage vs. Inductor Current (Chaotic Mode Operation)

A. Fundamental and Subharmonic Orbits

The *fundamental periodic* operation which is the most acceptable operation employed in practical power supplies. In this operation, waveforms repeat at the same rate *i.e.* after one cycle with the externally driving clock pulse. It is also known as "*Period–I operation*". The corresponding phase portrait is shown in Fig. 3 [1] which demonstrates the stable and periodic nature of the system. Similarly *period-two subharmonic* operation is shown in Fig. 4 [1] *i.e.* state variables repeat after *"2"* cycles, so it is a "*Period II operation*". It is worth noting that subharmonic operations have never been considered in the practical design of power supplies despite the fact that they are stable.

B. Chaotic Orbits

The phase portrait of chaotically operating circuit is shown in Fig. 5 [1]. The state variables *i.e.* inductor current and output capacitor voltage repeats after *"n"* times, so it is a "*Chaotic mode operation*". Conventional power supply designers have always banned this type of operation in their final products.

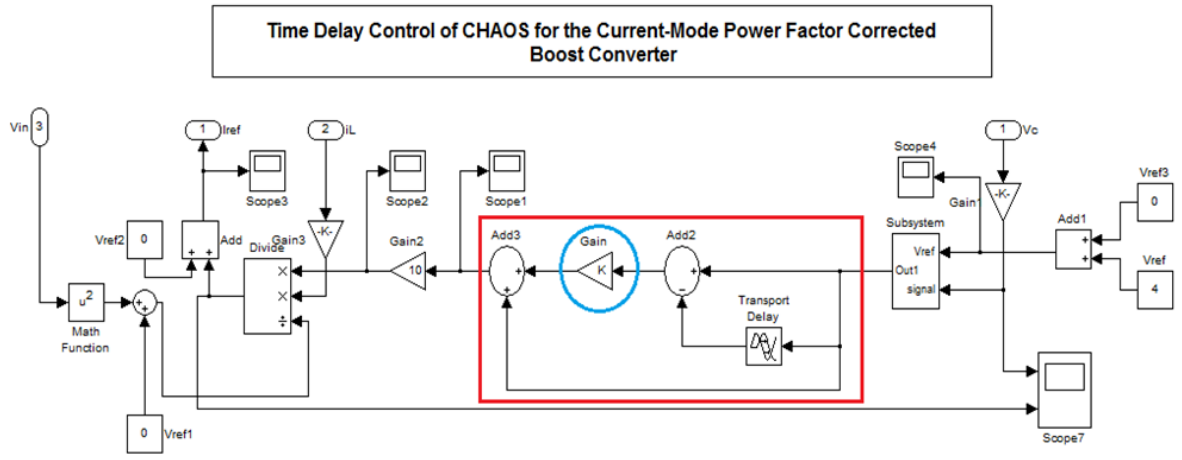

Fig. 6(a). MATLAB Model of Time Delay Feedback System *(TDS)* Control of Chaos of PFC Controller Block. [1]

BEFORE CONTROLLING CHAOS

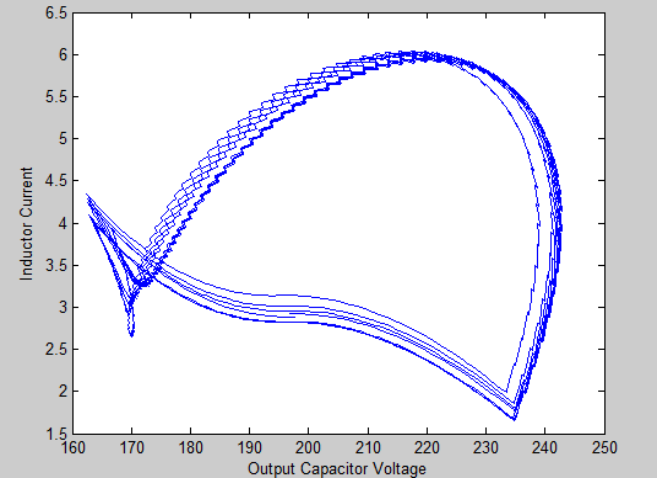

Fig. 6(b). Phase Portrait of Capacitor Voltage vs. Inductor Current before Controlling Chaos.

AFTER CONTROLLING CHAOS

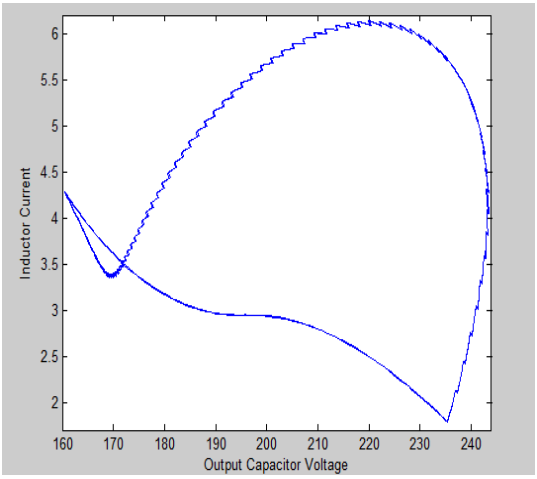

Fig. 7. Phase Portrait of Capacitor Voltage vs. Inductor Current after Controlling Chaos (K= 4).

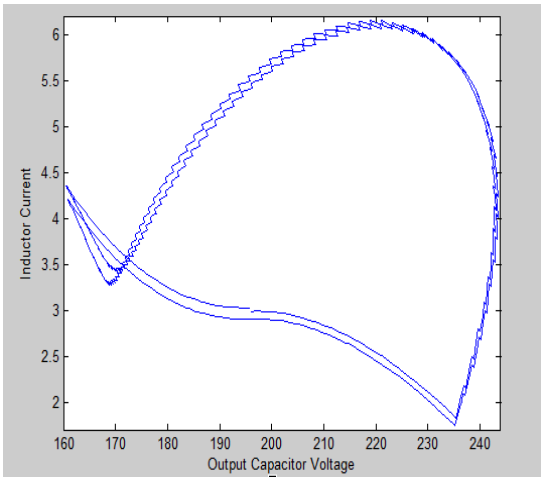

Fig. 8. Phase Portrait of Capacitor Voltage vs. Inductor Current after Controlling Chaos (K= 1).

VI. CONTROL OF CHAOS

Time Delay Feedback System *(TDS)* is picked up for controlling the Chaos. Our strategy to stabilize the UPO by modifying the reference current with a term proportional to the difference between a linear combination of the present and past states of the system. The Chaotic mode phase portrait is shown in Fig. 5; the Time Delay Feedback System is used for controlling the chaos which is marked as a square in Fig. 6 (a). The circular shape is denoted the gain K of the chaos controller (marked in Fig. 6 (a)). The gain K is varied and observes the phase-plane trajectories in Fig. 7 & 8 after controlling the chaos. *"Period I"* and *"Period II"* operation observe at K = 4 & 1 respectively.

VII. CONCLUSIONS

In this paper we describe the nonlinear phenomena like chaos of ac-dc current controlled power-factor-correction boost convertor. Here we have been investigated with considering the nonlinear model. The phase-plane-trajectories are observed by varying value of *load resistance R* where output capacitor voltage (v_C) and inductor current (i_L) are considered as state variables. The phase-portrait of output capacitor voltage (v_C) and inductor current (i_L) is going to *"period I"* to *"period II"* to *"chaotic-mode"* by increasing or decreasing the value of *load resistance R.* Chaotic phenomena are understood by multiple loops on phase-plane diagram. The most important point is to control the chaos and it is done by time delay feedback system *(TDS)*. We can control entire system in our desired region *i.e. "period I", "period II"* according to our demand. The simulation results and figures are also agreed with our statements.

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